

REMARKS

Claims 1-4 have been amended. No claims have been canceled or added. Accordingly, claims 1-4 are currently pending in the above-identified application.

35 U.S.C. §103

Claims 1-4 stand rejected under 35 U.S.C. §103(a) as being anticipated by Takeuchi et al in view of Sadd. This rejection is traversed as follows.

According to the present invention, each memory cell stores two bits of information. The cited references fail to disclose two charged storage regions (such as J12, J13) that are formed by a plurality of charged storage grains and that each store one bit of information such that each memory cell can store two bits of information.

According to the presently claimed invention, a first charge storage region is formed with a first set of plural charged storage grains in a vicinity of a source region. A second charge storage region J13 is formed with a second set of plural charge storage grains J10 arranged in vicinity of a drain region J8. Each of the first charged storage region and the second charged storage region stores one bit of

information, respectfully. As a result, each of the memory cells stores two bits of information.

The Examiner relies upon a newly cited reference to Sadd for disclosing a memory cell having a plural number of charge storage elements. Sadd discloses a memory cell that has a plurality of isolated storage elements 200 between a channel region and a control gate electrode 204 of source and drain regions 304. However, as shown in Figs. 4 and 5 and clearly described by Sadd, the memory cells are written to by hole (402) injection from all areas of the channel region and are deleted from by electron (502) injection from all areas of the channel region so that each of the memory cells stores only one bit of information using all of the isolated charge elements 200 (See Figs. 4 and 5, Column 5, lines 51-67 and Column 6, lines 56-67).

On the other hand, according to the presently claimed invention, first and second charge storage regions J12 and J13 are formed using first and second sets of plural charge storage grains J10 so that each of the first and second charge storage regions stores one bit of information. As a result, the memory cell can store two bits of information.

The deficiencies in Sadd are not overcome by resort to Takeuchi et al. Takeuchi et al discloses a multi-level

nonvolatile semiconductor memory device including a memory cell, a reference voltage generator and a level shifter (See Abstract). However, as shown in Figs. 14 and 26 and corresponding description, each of the memory cells stores two bits of information using four states (11, 10, 01 and 00) of threshold voltages.

On the other hand, each of the first charge storage region J12 and a second charge storage region J13 are constituted with first and second sets of plural charge storage grains arranged in the vicinity of a source region and drain region, respectively. In addition, each charge storage region stores one bit of information so that each memory cell can store two bits of information. This deficiency in Takeuchi et al is not overcome by resort to Sadd for the reasons mentioned above. As such, it is submitted that the pending claims patentably define the present invention over the cited art.

CONCLUSION

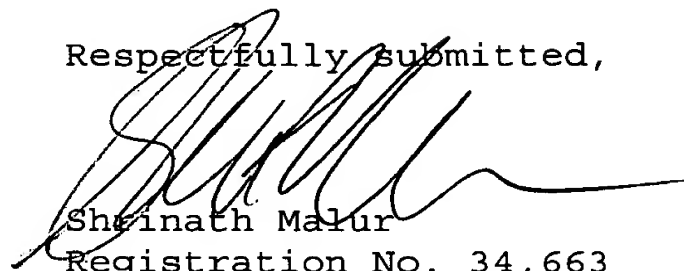
In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is

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now in condition for allowance. Accordingly, reconsideration and reexamination are respectfully requested.

Respectfully submitted,

A handwritten signature in dark ink, appearing to read 'Shrinath Malur', is written over the typed name.

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